[This question paper contains **4** printed pages.]

Your Roll No. .....

6607 **B**

B.Sc. (H) Computer Science / (II Sem.)

Paper 202 – COMPUTER SYSTEM ARCHITECTURE

(Admissions of 2001 and onwards)

Time : 3 *Hours* *Maximum Marks* : 75

(Write your Roll No. on the top immediately on receipt of this question paper.)

Attempt *All* questions.

State the assumptions made in your answers.

1. (*a*) Define fetch, decode and execute phases of an instruction cycle. State the sequence of micro-operations using register transfer statements. 6

   (*b*) A digital computer has a memory unit with a capacity of 16,384 words, 40 bits per word. The instruction code format consists of six bits for the operation part and fourteen bits for the address part (no mode bit). Two instructions are packed in one memory word and a 40-bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer. 4

2. (*a*) Formulate a mapping procedure that provides eight consecutive micro-operations for each routine of a

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basic computer. The opcode has six bits and the control memory has 2048 words. 3

(*b*) A control memory in a microprogrammed control unit has 4096 words of 24-bits each. Evaluate the following : 3

(*i*) Give the number of bits in CAR.

(*ii*) Specify the inputs to two MUX used in the system.

(*c*) Draw and explain the microprogrammed control organization. 4

3. (*a*) What are the characteristics of RISC and CISC processors ? How is a RISC processor better than a CISC processor ? Justify your answer. 3

(*b*) What is cache coherency ? Explain various approaches to maintain cache coherency in a multi-processor system. 4

(*c*) Let the address stored in program counter be X1. The instruction stored in X1 has an address part X2. The operand needed to execute the instruction is stored in the memory location X3. An index register contains X4. Illustrate the relationship between these

quantities if the addressing mode of the instruction is :

(*i*) indirect

(*ii*) relative

(*iii*) indexed. 3

4. (*a*) List and explain the different types of I/O commands received by an I/O processor during programmed I/O event. 5

(*b*) What design issues arise in implementing an interrupt driven I/O while handling multiple interrupts ? Explain any *two* technique adopted to resolve these issues. 5

5. (*a*) Show step by step multiplication process for $(-7)_{10} \times (-3)_{10}$ using Booth's algorithm. 6

(*b*) List and explain briefly the four methods of rounding the result of a floating point operation as given by IEEE standard. 4

6. (*a*) Determine the no. of clock cycles that it takes to process 200 tasks in a six-segment pipeline. 5

(*b*) List and describe the two dynamic approaches for branch prediction in a pipelining system. Which one is more advantageous and why ? 5

7. (*a*) Differentiate between LRU and LFU replacement algorithms used while caching. 2

(*b*) What is a loop buffer ? What are the benefits of using a loop buffer in a pipelining system ? 3

(*c*) If total memory space accessed by the CPU is 4096 × 16 bits, how many bits are required in its program counter (PC) and data register (DR) ? 2

(*d*) Draw the timing diagram assuming Sequence Counter (SC) is cleared to zero at timing signal T_4, if C_7 is active. 3

$$C_7T_4 : SC \leftarrow 0$$

(*e*) A set-associative cache memory consists of 64 lines (slots), divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory address and explain the set-associative mapping using a block diagram. 5